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10/759,072	01/20/2004	Makoto Onozawa	122.1577	3265

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EXAMINER	
LIE, ANGELA M	

ART UNIT	PAPER NUMBER
2821	

DATE MAILED: 06/06/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/759,072	ONOZAWA ET AL.	
	Examiner	Art Unit	
	Angela M. Lie	2821	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 January 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-51* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,12-13,22,37,43-46,50 and 51* is/are rejected.

7)☒ Claim(s) *4-11,14-21,23-36,38-42 and 47-49* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 January 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *01/20/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 12-13, 22, 37, 43-46 and 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Onozawa et al (US 20020097203) in the view of Carson et al (US 20010055258).

As to claim 1, Onozawa et al teach a capacitive load driving circuit comprising: an input terminal (Figure 11A, element Iin), an amplifying circuit for amplifying a drive control signal obtained through the front-edge delay circuit and the back-edge delay circuit (Figure 10 element 42), and an output switch device which is driven by the amplifying circuit (Figure 6 element SW4). Onozawa et al do not explicitly state that phase tuning circuit (Figure 10 element 49) comprises a back-edge delay circuit for delaying a back edge of the input signal and a back-edge delay circuit for delaying a back edge of the input signal. Carson et al teach the circuit which comprises rising edge delay generator (Figure 11 element 224) and falling edge delay generator (Figure 11 element 228). It would have been obvious to one of the ordinary skill in the art during the time when the invention was made to incorporate Carson's et al rising and falling edge generators as well as rising and falling edge detectors into capacitive load driving circuit (in the place of phase tuning circuit, figure 10 element 49) as taught by Onozawa

et al because regulating rising and falling edge of the pulse would generate an optimized modulation signal (accurate). This would prevent rising and falling edges in the output signal from overlapping, which in result would prevent from possible errors caused by misread signal. Furthermore delay control reduces a penetration current (JP 2001358570).

As to claim 2, Carson et al teach the circuit wherein the front-edge delay circuit is rising edge delay circuit for delaying a rising edge (Figure 11, elements 216 and 224, since there is the rising edge detector circuit (216), if the input signal has a front edge being rising edge, the rising edge delay circuit (224) would correspond to the front edge) of the input signal; and the back-edge delay circuit is a falling edge delay circuit for delaying a falling edge of the input signal (Figure 11, elements 218 and 228, if the input signal has a back edge being falling edge, the falling edge delay circuit (224) would correspond to the back edge).

As to claim 3, Carson et al teach the circuit wherein the input signal is a positive polarity pulse signal (Figure 5, positive polarity pulse is understood as a pulse which has positive values of voltages, therefore this pulse starts from rising edge as shown in the figure).

As to claim 12, Carson et al teach the circuit wherein the front-edge delay circuit is falling edge delay circuit for delaying a falling edge (Figure 11, elements 218 and 228, since there is the falling edge detector circuit (218), if the input signal has a front edge being falling edge, the falling edge delay circuit (228) would correspond to the front edge) of the input signal; and the back-edge delay circuit is a rising edge delay circuit

for delaying a rising edge of the input signal (Figure 11, elements 216 and 224, if the input signal has a back edge being rising edge, the rising edge delay circuit (224) would correspond to the back edge).

As to claim 13, the circuit as taught by Carson et al (i.e. rising and falling edge delay circuit) is capable of utilizing a negative polarity pulse signal.

As to claim 22, Carson et al teach the circuit wherein the front-edge delay circuit is a first monostable multivibrator (Figure 11 elements 216 and 224) which is triggered by the front edge of the input signal (where the front edge would be a rising edge); and the back-edge delay circuit is a second monostable multivibrator (Figure 11 elements 218 and 228) which is triggered by the back edge of the input signal (where the back edge would be a falling edge), and wherein the drive control signal (Figure 11 element 262) is generated by combining an output signal of the first monostable multivibrator with an output of the second monostable multivibrator.

As to claim 37, Onozawa et al teach a capacitive load driving circuit comprising: an input terminal (Figure 11A element Iin), an amplifying circuit for amplifying the drive control signal (Figure 10 element 42), an output switch device which is driven by the amplifying circuit (Figure 6 element 42). Onozawa et al do not teach explicitly a front-edge delay circuit for delaying a front edge of an input signal input via the input terminal; a pulse width adjusting circuit for generating a drive control signal having a prescribed pulse width from a delayed signal obtained through the front-edge delay circuit. Carson et al teach a front edge delay circuit comprising a rising edge detector (Figure 11 element 216), rising edge delay table (Figure 11 element 344, for prescribed pulse

width) and rising edge delay generator (Figure 11 element 224, for delaying front edge signal). It would have been obvious to one of the ordinary skill in the art during the time when the invention was made to incorporate Carson's et al front edge delay circuit into Onozawa et al capacitive load driving circuit in the place of phase tuning circuit (Figure 10 element 49) because Carson's delay circuit could generate optimized modulation signal (accurate). This would prevent rising and falling edges in the output signal from overlapping, which in result would prevent from possible errors caused by misread signal. Furthermore delay control reduces a penetration current (JP 2001358570).

As to claim 43, Carson et al teach a circuit wherein the front-edge delay circuit is a rising edge delay circuit for delaying a rising edge of the input signal (Figure 11 elements 216, 344 and 224); and the pulse width adjusting circuit is a monostable multivibrator (rising edge delay generator (224 connected with pulse width adjustment (344)) is controlled by rising edge detector (216), so it can be in on or off mode).

As to claim 44, Carson et al teach a circuit wherein the input signal is a positive polarity pulse signal (Figure 5).

As to claim 45, Carson et al teach circuit wherein the front-edge delay circuit is a falling edge delay circuit for delaying a falling edge of the input signal (since circuit as taught by Carson et al has rising and falling edge detector (216 and 218), it is capable of receiving a negative pulse where the front edge is a falling edge, once the falling edge is detected by element 218, falling edge delay generator can be turned on and adjust the front edge of the pulse); and the pulse width adjusting circuit (Figure 11 element 348) is a monostable multivibrator (element 348 and 228 are connected to the

falling edge delay generator and the falling edge generator is controlled by falling edge detector, therefore it ultimately can be in on and off position).

As to claim 46, the circuit as taught by Carson et al (i.e. rising and falling edge delay circuit) is capable of utilizing a negative polarity pulse signal.

As to claim 50, Onozawa et al teach a plasma display apparatus comprising: a plurality of x electrodes (Figure 17, element X), a plurality of Y electrodes (Figure 17 element Yn) which are arranged substantially parallel to the plurality of X electrodes (Figure 18A elements X and Y), and which produce a discharge between the plurality of Y electrodes and the plurality of X electrodes (paragraph 5); an X-electrode driving circuit which applies a discharge voltage to the plurality of X electrodes, a Y-electrode driving circuit which applies a discharge voltage to the plurality of Y electrodes, and wherein the X-electrode driving circuit or the Y-electrode driving circuit is constructed using capacitive load driving circuit, wherein the capacitive load driving circuit (paragraphs 3 and 5) comprises: an input terminal (Figure 11A element Iin), an amplifying circuit for amplifying a drive control signal obtained though the front-edge delay circuit and the back-edge delay circuit (Figure 10 element 41), and an output switch device which is driven by the amplifying circuit (Figure 6 element SW4). Onozawa et al do not teach a front-edge delay circuit for delaying a front edge of an input signal input via the input terminal and a back-edge delay circuit for delaying a back edge of the input signal. Carson et al teach the circuit which comprises rising edge delay generator (Figure 11 element 224) and falling edge delay generator (Figure 11 element 228). It would have been obvious to one of the ordinary skill in the art during

the time when the invention was made to incorporate Carson's et al rising and falling edge generators as well as rising and falling edge detectors into capacitive load driving circuit (in the place of phase tuning circuit, figure 10 element 49) as taught by Onozawa et al because regulating rising and falling edge of the pulse would generate an optimized modulation signal (accurate). This would prevent rising and falling edges in the output signal from overlapping, which in result would prevent from possible errors caused by misread signal. Furthermore delay control reduces a penetration current (JP 2001358570).

As to claim 51, Onozawa et al teach a plasma display apparatus comprising: a plurality of x electrodes (Figure 17, element X), a plurality of Y electrodes (Figure 17 element Yn) which are arranged substantially parallel to the plurality of X electrodes (Figure 18A elements X and Y), and which produce a discharge between the plurality of Y electrodes and the plurality of X electrodes (paragraph 5); an X-electrode driving circuit which applies a discharge voltage to the plurality of X electrodes, a Y-electrode driving circuit which applies a discharge voltage to the plurality of Y electrodes, and wherein the X-electrode driving circuit or the Y-electrode driving circuit is constructed using capacitive load driving circuit, wherein the capacitive load driving circuit (paragraphs 3 and 5) comprises: an input terminal (Figure 11A element Iin), an amplifying circuit for amplifying a drive control signal obtained though the front-edge delay circuit and the back-edge delay circuit (Figure 10 element 41), and an output switch device which is driven by the amplifying circuit (Figure 6 element SW4). Onozawa et al do not teach front-edge delay circuit for delaying a front edge of an input

signal input via the input terminal and a pulse width adjusting circuit for generating a drive control signal having a prescribed pulse width from a delayed signal obtained through the front-edge delay circuit. Carson et al teach the circuit comprising front-edge delay circuit (Figure 11 elements 224 or 228 depending on type of the pulse i.e. negative or positive) and pulse width adjusting circuit (Figure 11 element 348) having a prescribed pulse width from a delayed signal obtained trough the front-edge delay circuit (Figure 11 elements 206 and 220). It would have been obvious to one of the ordinary skill in the art during the time when the invention was made to incorporate a front edge delay circuit and a pulse width adjusting circuit as taught by Carson et al because exact regulating rising and falling edge of the pulse would generate an optimized modulation signal (accurate). This would prevent rising and falling edges in the output signal from overlapping, which in result would prevent from possible errors caused by misread signal. Furthermore delay control reduces a penetration current (JP 2001358570).

3. Claims 4-11, 14-21, 23-36, 38-42 and 47-49 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Allowable Subject Matter

4. The following is a statement of reasons for the indication of allowable subject matter:

As to claim 4, the prior art failed to teach the capacitive load driving circuit wherein the rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, where the circuit operates in the manner as taught in claim 4.

As to claims 5-7, those claims could be allowable by the virtue of their dependency on claim 4.

As to claim 8, the prior art failed to teach the capacitive load driving circuit wherein the falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, where the circuit operates in the manner as taught in claim 8.

As to claims 9-11, those claims could be allowable by the virtue of their dependency on claim 8.

As to claim 14, the prior art failed to teach the capacitive load driving circuit wherein the rising edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, where the circuit operates in manner as taught in claim 14.

As to claims 15-17, those claims could be allowable by the virtue of their dependency on claim 14.

As to claim 18, the prior art failed to teach the capacitive load driving circuit wherein the falling edge delay circuit comprises a capacitive element and a parallel circuit of a resistive element and a switch element, where the circuit operates in the manner as taught in claim 18.

As to claims 19-21, those claims could be allowable by the virtue of their dependency on claim 18.

As to claim 23, the prior art failed to teach the capacitive load driving circuit, wherein the front-edge delay circuit comprises a first capacitive element and a first series circuit having a first resistive element and a first switch element; and the back edge delay circuit comprising a second capacitive element and a second series circuit having a second resistive element and second switch element, wherein the first and second series are connected in parallel.

As to claims 24-26, those claims could be allowable by the virtue of their dependency on claim 23.

As to claim 27, the prior art failed to teach the capacitive load driving circuit wherein the front-edge delay circuit comprises a first resistive element and a first resistive element and a first capacitive element, the back-edge delay circuit comprises a second capacitive element and a series circuit having a second resistive element and a switch element and, wherein the first resistive element and the series circuit are connected in parallel.

As to claims 28-31, those claims could be allowable by the virtue of their dependency o claim 27.

As to claim 32, the prior art failed to teach the capacitive load driving circuit wherein the front-edge delay circuit comprises a first counter which starts to count a clock signal from the front edge of the input signal and the back-edge delay circuit comprising a second counter which starts to count the clock signal from the back edge

of the input signal, and wherein the delay time of the front edge is adjusted by varying a delay time of the front edge is adjusted by varying a count value of the first counter, and delay time of the back edge is adjusted by varying a count value of the second counter.

As to claim 33, this claim could be allowable by the virtue of its dependency on claim 32.

As to claim 34, the prior art failed to teach the capacitive load driving circuit wherein the capacitive load driving circuit comprises a first and a second capacitive load driving circuit; a first and a second capacitive load driving circuit, a first output switch device in the first capacitive load driving circuit is connected between power line and a capacitive load; and a second output switch device in the second capacitive load and a reference voltage.

As to claims 35-36, those claims could be allowable by the virtue of their dependency on claim 34.

As to claim 38, the prior art failed to teach a capacitive load driving circuit as disclosed in claim 37 and further comprising front-edge delay circuit comprising a resistive element and capacitive element; and the pulse width adjusting circuit being a monostable multivibrator.

As to claims 39-41, those claims could be allowable by the virtue of their dependency on claim 38.

As to claim 42, the prior art failed to teach the capacitive load driving circuit wherein the front-edge delay circuit is a first counter for counting a clock signal; and the pulse width adjusting circuit is a second counter for counting the clock signal, and

wherein the delay time of the input signal is adjusted by varying a count value of the first counter, and the pulse width of the drive control signal is adjusted by varying a count value of the second counter.

As to claim 47, the prior art failed to teach the capacitive load driving circuit wherein the capacitive load driving circuit comprises a first and a second capacitive load driving circuit, a first output switch device in the first capacitive load driving circuit is connected between a power line and a capacitive load; and a second output switch device in the second capacitive load driving circuit is connected between the capacitive load and a referenc-e voltage.

As to claims 48-49, those could be allowable by the virtue of their dependency on claim 47.

The Prior Art

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

- US 6329980 discloses a driving circuit for display device
- US 5541452 discloses an image device and its driving circuit
- US 20020054001 discloses a driving method and driving circuit of plasma display panel
- US 5311169 discloses a method and apparatus for driving capacitive display device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Angela M. Lie whose telephone number is 571-272-8445. The examiner can normally be reached on M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Don Wong can be reached on 571-272-1834. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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Don Wong
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Technology Ce